Design of Field Programmable Gate Array(FPGA) based data acquisition system for avionics applications

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Abstract— Present data acquisition systems for avionics applications uses microcontrollers with external filters to process the digitized data. To minimize the use of external components, the digital filter itself is implemented in FPGA for this work. Moreover, microcontroller based systems may get affected in adverse conditions like high radiation environments and high temperature variations. To resolve this issue, an FPGA based data acquisition system for space application is proposed. FPGA's can be used for reliable communication in high radiation environments and are available in extended industrial grade/space grades.The Flash-based FPGA used for this work provides reprogrammability.This paper discusses the system concepts for implementing a wireless FPGA based data acquisition unit. The study involves the digitization of analog sensor channels, processing the digitized data, transfer of processed data between master and slave FPGA's. There are slave nodes in which data is processed and one master node in which data is finally received and stored. The slaves communicate with the master node over one or more wireless interface. In this manner the slaves and the master communicate in a multi-drop network. The work involves simulation in MATLAB, HDL coding & simulation, prototype development, system interfacing, assembly and testing. The simulation results are shown and the future course of action is identified.

Index Terms— analog to digital conversion, avionics, data acquisition, decimation, FPGA, microcontroller, transceivers

1 Introduction

Conventional microcontroller based data acquisition systems have limited operating environments. Suitable protection is required against adverse radiation environments. On the contrary, FPGA's have been designed to survive high radiation and temperature effects without affecting its functionality[1].Moreover, true logic implementation is faster compared to processor logic. In the proposed architecture, the digitized data is digitally filtered within the FPGA, which is an added advantage. Thus it helps to reduce the number of external components involved. As the processing and communication modules are all implemented in one single FPGA, maximum utilization of FPGA is ensured. A reliable data transmission to the user can be ensured via wired and wireless interfaces.

The flash-based FPGA's used for this work provides a unique combination of re-programmability. Unlike SRAM-based FPGA's, flash-based FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. The device will not have to be reloaded with the programming file (STAPL) when system power is restored. Once it is programmed, the flash cell configuration element of Flash FPGAs cannot be altered by high-energy particles like neutrons and is therefore immune to them [2].

Implementation of FPGA based data acquisition system involves the implementation of a master node for storing the data and salve node for processing the data. In a slave node, the sensor data is first filtered using an analog filter and then it is digitized using an ADC which is to be interfaced with the FPGA. In FPGA, the digitized data is downsampled to the required sampling frequency using a decimator implemented in it. The decimator implemented is a CIC decimator. This data is then collected and stored in master.

2 Related Study

The analog sensor output must be passed through an analog to digital convertor (ADC) before passing into the FPGA. The input continuous time signal gets sampled at periodic intervals. The method used here is to sample the signal in a much higher than Nyquist rate, then digitizing in a fast low resolution ADC and then decimate this digital output to the Nyquist rate. The problems of sharp cut off required for analog anti-aliasing filter is reduced here, resulting in simple filter structure which is built using low precision analog components. Oversampling at ADC helps to avoid aliasing, improves resolution and decreases the noise power in the signal band of interest[3]. A successive approximation ADC can be used which has a speed limit up to 0. 5Msps.

Down sampling at FPGA is to reduce the sampling rate of the signal to the required frequency. It reduces the data rate or size of the data. While reducing sampling rate, sampling theorem should be satisfied to avoid aliasing. So to ensure this, an analog low pass filter is used as anti-aliasing filter at the input to reduce the band width of signal before down sampling. If the oversampled signal is already nyquist compliant, then downsampling can be done without any filtering [4].

Cascaded Integrator comb filters (CIC) can be used to make the transition between high & low f_s (Sampling frequency). They use conventional filters at low f_s to shape or clean up

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the frequency response, which is a sinc function [5]. Advantages of using CIC filters for decimation are no multipliers are required, no storage for filter coefficients are needed and can be used for wide range of rate change factors [6]. So a CIC decimator is implemented in the FPGA for this work.
A length-D ,Mth order comb filter has Transfer Function,

$$H(z) = \left(\frac{1 - z^{-D}}{1 - z^{-1}} \right)^{M} \quad (1)$$

In time domain, the response of the filter can be represented as shown in the equation below,

$$y(n) = \frac{x(n) - x(n-m) + y(n-1)M}{M} \quad (2)$$

Where M is decimation factor & n is no. of samples
Response of the filter in frequency domain can be represented as shown in the equation below,

$$h(e^{jw}) = \left(\frac{\sin \frac{wm}{2}}{M \times \sin \frac{w}{2}} \right)^{k} \quad (3)$$

where k is the order & $w = \frac{2 \times \Pi \times f}{f_s}$, f_s is the sampling frequency [3].

The CIC decimator can be implemented in MATLAB and the HDL(Hardware Description Language) code can be generated using the HDL generator available with MATLAB toolkit. But the generated code is large and complex compared to the hand written code. Also, readability, traceability and optimization are challenging tasks for the matlab generated code.

UART(Universal Asynchronous Receiver Transmitter) is the wired communication interface implemented for this work. It can be used with communication standards such as RS485, RS232, RS422. At the destination, a receiver UART reassembles the bits into complete byte[7]. RS485 allows multiple devices to communicate at half duplex on a single pair of wires at distances up to 1200meters. Devices are addressable allowing each device to communicate independently.Speed of differential bus interfaces RS422, RS485, is superior to the single ended versions RS232 & RS423 and they have higher noise immunity. There is a maximum slew rate for RS232 & 423. It limits the maximum communication speed on line. Maximum allowed voltage range for all interfaces are in same range, but signal level is lower for faster interfaces. So RS485 can be used where a severe ground level shift of several bits is there, also high bit rates are possible because transition between logic 0 & 1 is only few 100mv's [8].

SPI(Serial Peripheral Device) is the wireless communication interface between the FPGA's and various peripherals(ADC's, transceivers) in this work. The FPGA acts as the SPI master providing the clock for initiating communication with the peripherals, which act as SPI slaves. Individual peripherals are activated for SPI data transfer by appropriate chip select signals. Clock polarity and clock phase determine the edges of the clock signal on which the data are driven and sampled. The master and slave must use the same parameter pair values to communicate [9].

Cellular protocols are available for transmitting voice and data over the well-established infrastructure of cellular telephone networks. Bluetooth is used for low power applications with short range and moderate data rate at 2.4Ghz. It can address a maximum of 7 devices. Wifi can be used for high data rate, high range applications. But, they have significant power at their disposal as these devices are powered from the mains. They are also susceptible to multipath problems, as the modulation used is DSSS(Direct sequence Spread Spectrum). Zigbee/ IEEE 802.15.4 are suitable for low data-rate applications. The maximum data rate achievable is 250 kbps at 2.4 GHz. It has an address space for 2^{16} devices. RFID is well suited for short range, low power systems. These protocols have significant overheads and the actual, transmitted data payload is small. For this work, the system is built for a specific application, which requires high speeds, long ranges, low power and minimum overheads.

For wireless communication, the frequency required for reliable data transmission has to be selected. The attenuation of signal strength with distance by absorption in the ground is lower at lower frequencies. As frequency increases, the signal is absorbed more by physical objects (atmospheric moisture, trees, buildings, etc.). For constant power, the range decreases because the signal losses increase with increasing frequency. This is a fundamental result of the Friis Transmission Equation [10]. This means that for antennas with specified gains, the energy transfer will be highest at lower frequencies. Friis Transmission Equation says that the path loss is higher for higher frequencies.. With high data rate the probability of collision incidences is greatly reduced because of short transmission time, which also reduces overall power consumption.

For the wireless data transmission, the modulation technique used is Minimum Frequency Shift Keying (MFSK). In MSK, the modulating data signal changes the frequency of the signal. Phase discontinuities are avoided because the frequency changes occur at the carrier zero crossing points[11].

3 Generalized Block Diagram

The proposed system implements a bus controller that communicates with multiple remote terminals. The bus controller is the master node here and the remote terminals are the slave nodes. The master and the slave nodes are controlled using master and slave FPGA's separately for each node. The master data acquisition unit's terminal, interfaces with the multiple slave data acquisition unit's terminals. Figure 1 shows the generalized block diagram of the proposed model.

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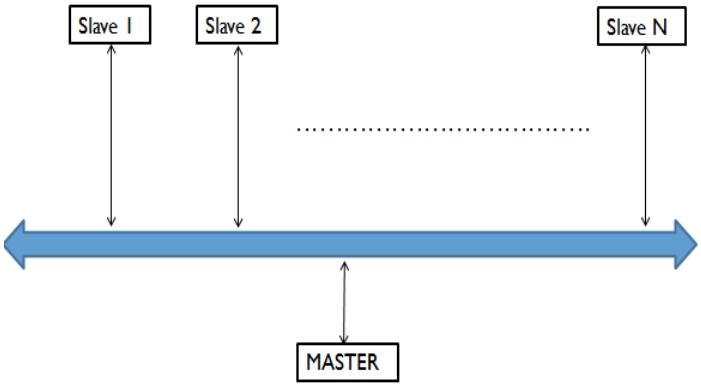

Figure 1.Generalised block diagram for the proposed system.

4 Implementation of Slave Node

The sensors that need to be monitored are connected to the slave node. In the front end a simple Resistor-Capacitor (RC) Low Pass Filter (LPF) is used to filter off high frequency components. A 12-bit successive approximation ADC is used for each channel. A CIC decimation filter for digital filtering and an SPI module for transferring the data are implemented in FPGA. These are to be interfaced to the ADC and RF transceivers. Here FPGA acts as the SPI master which generates the clock for the SPI slave and RF transceiver acts as the SPI slave. A voltage level translator is used to regulate the I/O voltage to the IC's within the package. A check out interface can be used for lab-level testing and verification. Figure 2 shows the implementation of the system's slave node.

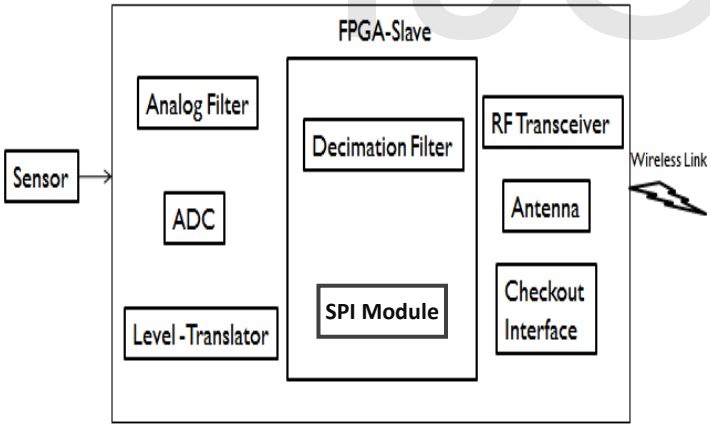

Figure 2. Implementation of Slave node for data acquisition system.

5 Implementation of Master Node

The FPGA is programmed with the UART module for wired interface, apart from the SPI module, for wireless interface. Data from the slaves received via the wireless interface is stored in the memory and given out when requested by the end user via the wired RS485 link. This can be obtained at any end device which is connected to the RS485 link. The RF and the power systems remain similar to slave node. Figure 3 shows the implementation of the system's master node.

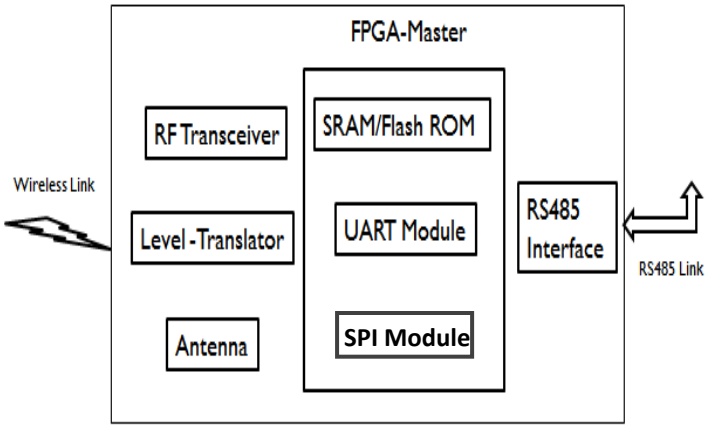

Figure 3. Implementation of Master node for data acquisition system.

6 Component Selection

Apart from FPGA, the components required are Analog to digital convertor, transceivers and level translator. For wired communication with the end user RS485 standard is implemented. Therefore, the transceiver used is Max3443/Max485 [9]. The voltage level translator used in this work is 74LVC4245 which can be used to shift the voltages from 2.7-3.6 to 4.5-5.5 and vice versa[12].

The ADC's available in extended industrial grade/space grade temperature ranges are, AD574A, AD7892S, AD9042S, AD10242, AD10200, AD674, AD872, AD1671. Among this, AD7892, AD9042S and AD10200 operates from single supply voltage. AD10200 and AD9042S are operating at very high data rates such as 105Msps and 41Msps respectively. They are made for specific applications like medical imaging. For the proposed application AD7892 is the suitable ADC which has a speed of 500ksps. It is a 12-bit Successive Approximation ADC that operates from a single +5 V supply [13]. It allows both serial and parallel connection to a controller [14].

The transceivers available in space grade temperatures and in acceptable data rates are CC1100, CC1101, CC2500, CC2420. CC1101, CC1100and CC2500 are having the highest data rates. As frequency decreases, range increases but antenna size increases. The lowest frequency is for CC1100 / CC1101 which translates to longer range. It is a trade-off between data rate, range and antenna size. As data rate decreases, range can be increased but the energy consumption increases [15]. CC1101 is a sub-1 GHz transceiver for low power wireless applications which can operate at 315/433/868/915 MHz frequency bands. At 915 MHz, it can operate at data rates upto 600kbps with receiver sensitivity upto -90dbm and can provide the maximum possible range. It can be controlled via an SPI interface [16]. These parameters made CC11101 the most suitable RF transceiver for the proposed work.

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7 Protocol Implementation

The master node communicates with multiple slaves using a common frame format. An M bit address send by the master node will be followed by an N bit data transfer. The master node sends the address of the slave from which the data is required. Upon reception of address, the slave nodes check for match in the address and only the slave whose address matches, responds by sending the processed data. The master node buffers this data from the slave, to its memory. Apart from that the SPI master should send an 8 bit command word to the SPI slave, which initiates the N-bit data transfer. This command word is used to select the receive and transmit registers for reading and writing data. All the slave nodes are by default in the listening mode. All devices communicate over a common frequency. Time division Multiplexing is adopted for accessing the slave nodes. When the master node is asked to output the data by the end user, it transmits the latest data available with it via the RS485 link to the end device to which it is connected. The master node matches the speed of RS485 bus at one end and the wireless network at the other end.

8 System Implementation

The different modules to be implemented in ProASIC3E FPGA, are programmed in libero IDE[17] using VHDL. The sinc filter is implemented in MATLAB to see the filter response at different filter orders. The decimation filter is then programed in VHDL and simulated. The numeric standard[18] is used for type conversions. Finite state machines[19] are used for programming both filter and UART modules as shown in figure 4, 5 & 6. Similarly, the SPI-Master and SPI-Slave modules are programmed for wireless communication. The synthesizable codes are then hard coded into the ProASIC3E FPGA using the Flashpro 4 programmer [2]. The codes are adjusted to match the speed of wired and wireless transceivers. After integrating the codes and implementing it into the FPGA, the ADC and the transceivers are interfaced to the FPGA with the help of level translators. Finally, the Resistor-Capacitor filter design completes the system implementation. The sensors can be connected and the results can be verified using the checkout interface. For both master and the slaves, ProASIC3E FPGA is used.

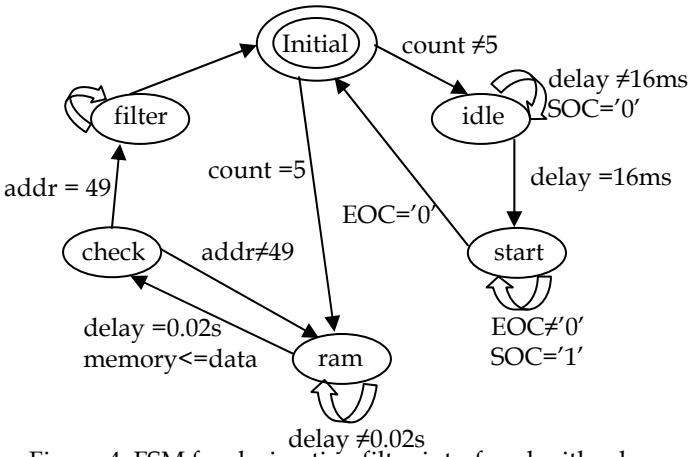

Figure 4. FSM for decimation filter interfaced with adc

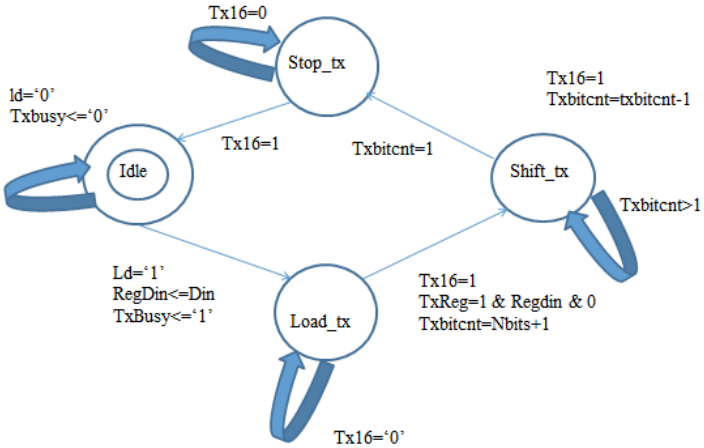

Figure 5. FSM for UART transmitter module

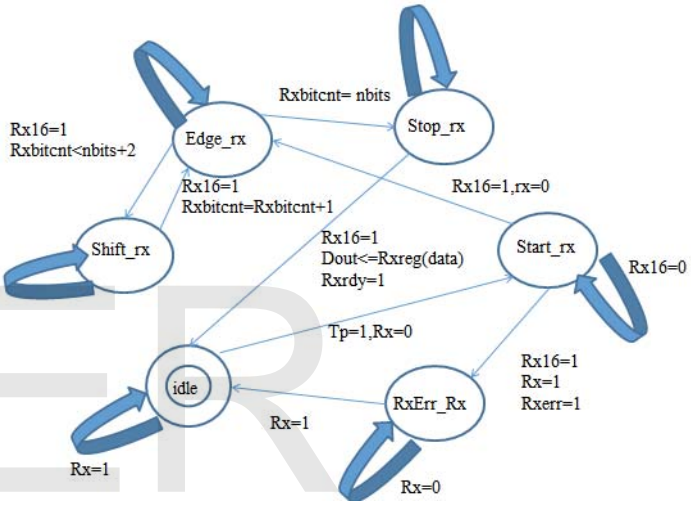

Figure 6. FSM for UART receiver module

9 Simulation Results

- Figure 7 shows the filter response of sinc filter in MATLAB for different orders.

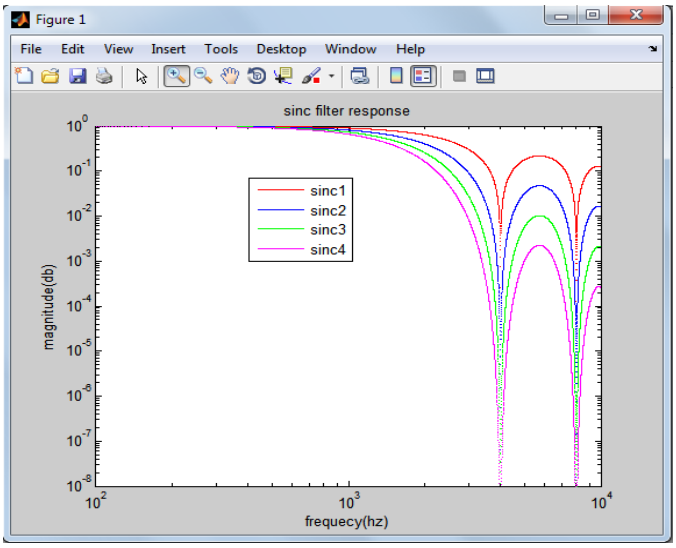

Figure 7. MATLAB filter response for the filter.

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- Figure 8 shows the simulation result for the filter implemented in libero IDE and the table 1. gives the inputs and outputs for the simulation result in figure 5.

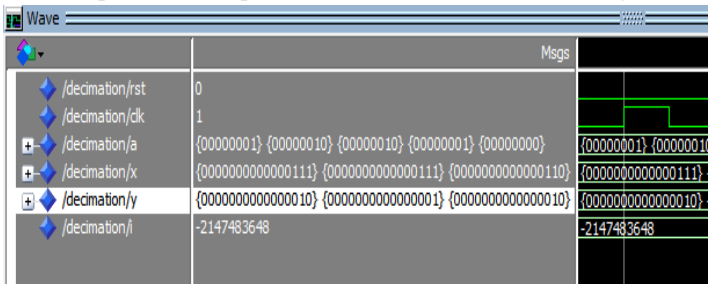

Figure 8. Simulation result of the filter.

Table 1. Input vs Output for the filter

Input (X)	Output (Y)
100	01
101	
110	10
111	
111	10
100	
101	01
110	
111	10
111	

- Figure 9 shows the simulation result for the UART module implemented.

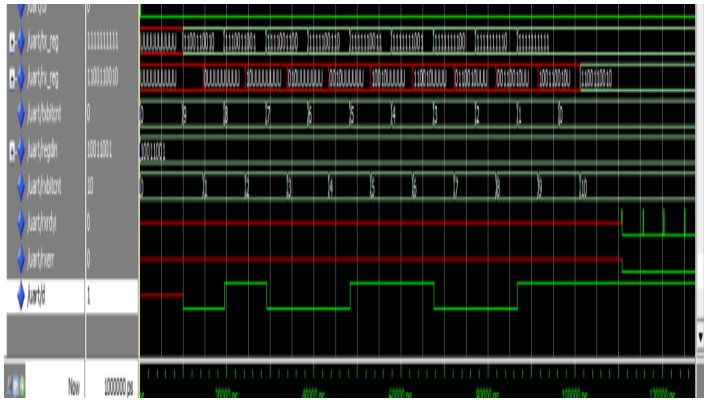

Figure 9. Simulation result of the UART module

- Figure 10 shows the simulation result for the SPI-Master module.

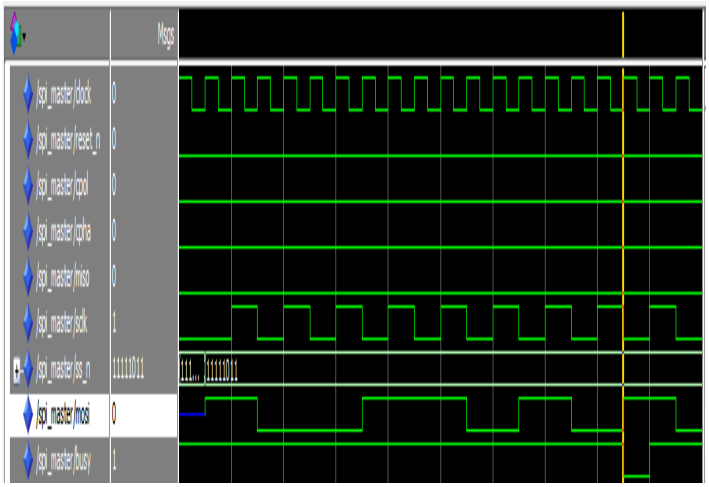

Figure 10. Simulation result of the SPI-master module

- Figure 11 shows the result of UART implemented in FPGA as seen in the CRO.

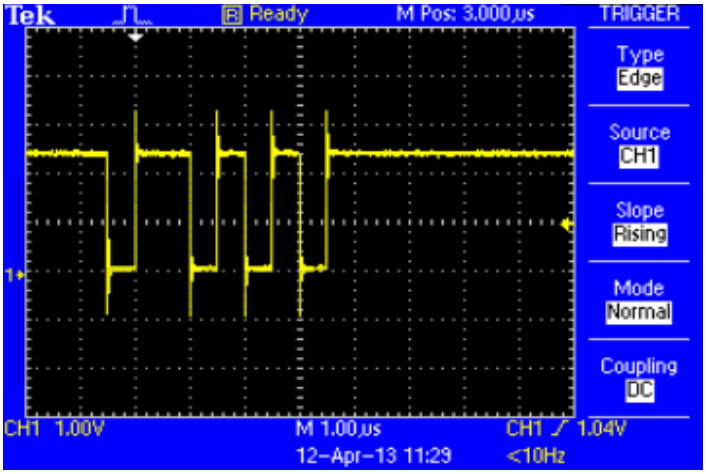

Figure 11. Output of UART as seen in CRO

- Figure 12 shows the result of SPI-Master implemented in FPGA as seen in the CRO.

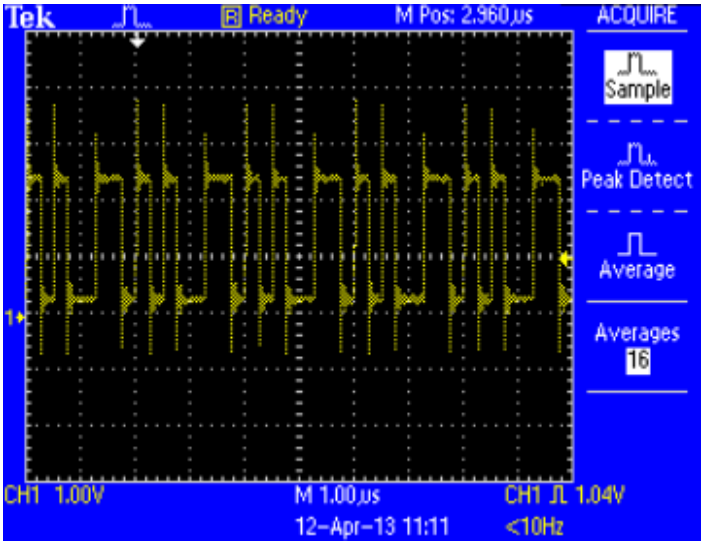

Figure 12. Output of SPI-Master as seen CRO

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10 Discussions

- Filter response in Figure 7 shows that the stop band attenuation improves as the order of the filter increases. So a higher order sinc filter is preferred for improved filter response.
- Input values from ADC are collected and stored in memory which is processed using the filter implemented in FPGA. The output for 10 input samples is as shown in the simulation window of figure 8. The downsampling rate is user definable. Here, it is taken as 2. While implementing filter in VHDL, problems like register overflow may occur. This can be solved by partial windownig.
- The input to the UART module is the processed signal which is transmitted from the FPGA slave and received at the FPGA master via the SPI interface. The data is received at the UART receiver and is transmitted via the serial output line. The data output can be seen in the 'd' line as highlighted in the figure 9. The data transmitted is "10011001" along with a start bit at the beginning and stop bit at the end.
- The SPI master output from the FPGA master can be seen in the MOSI line as highlighted in the simulation window of figure 10. This output will be received by the SPI slave at the FPGA slave nodes. According to the match in address sent by the master node, the corresponding FPGA slave responds by sending the processed data. The data transmitted is "10011010".
- The UART code is modified to make the data rate to 2Mbps to match with the speed of the transceiver. The FPGA gives the output data in the selected data rate. The data transmitted is "11010101". The output is given to a CRO, which displays the result as shown in figure 11.
- The SPI program is modified by making the SPI clock frequency to 4Mhz inorder to match with the frequency of the RF transceiver. The data transmitted is "10011010" in continuous mode. The output from MOSI line is given to CRO and the output in tuned clock frequency is displayed as shown in figure 12.

All the codes are integrated into a single project. The selected ADC is interfaced with the FPGA after calibration. The ADC is calibrated with the outputs obtained, and the calibration curve is obtained with minimum errors as shown in figure 13. The selected transceivers are interfaced with the FPGA for completing the wired and wireless interfaces. Thus the modules which are implemented and tested separately are all assembled. With the sensor and the RC filter at the front end of slave nodes, the system is complete for testing. The proposed system should undergo a series of tests before it can be used for space applications.

Voltage	Digital Output	Hex2dec	Predicted	Error	%Error
1	97	151	143.77	-7.23	0.353
2	19A	410	356.87	-53.13	2.594
3	240	576	569.97	-6.03	0.294
4	300	768	783.07	15.07	0.736
5	400	1024	996.17	-27.83	1.359
6	4C1	1217	1209.27	-7.73	0.377
7	563	1379	1422.37	43.37	2.118
8	65B	1627	1635.47	8.47	0.414
9	700	1792	1848.57	56.57	2.762
10	7FD	2045	2061.67	16.67	0.814
				Linearity	2.762 %

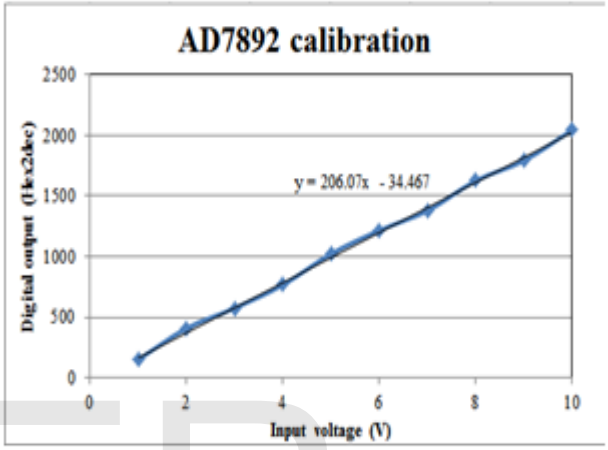

Figure 13. ADC Calibration

11 Future Scope

As the present system uses devices that operate at same frequency, interference problems such as line-holding by a single device may occur. To reduce such problems and to have increased reliability in communication, the master may be made to hop between the different frequencies that the slaves are programmed to. In such cases, channel spacing required will be more to prevent RF interference and the master will take additional time to switch and settle at each different frequencies.

The proposed system can be integrated with large bus control systems as one of its remote terminals. The master node can be one off the remote terminals which interfaces with multiple wireless slaves. In this wireless network, the master will act as secondary bus controller and the slaves as secondary remote terminals.

11 Conclusion

The proposed FPGA based data acquisition system is designed for space applications. The system can be integrated with other units for avionics applications. It ensures a reliable way of collecting, processing and transferring data. The analog input can be a sensor output, EEG/ECG or any other signal which needs to be monitored. This work can be modified suitably and can be used for manned missions, where it can be used to monitor the astronaut's health parameters.The work is underway for the implementation of the system for space applica-

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